

| L Number | Hits | Search Text   | DB                         | Time stamp       |
|----------|------|---|----------------------------|------------------|
| 6        | 1    | (cypress adj semiconductor) and (dummy with trenches)   | USPAT; US-PGPUB            | 2004/09/16 14:06 |
| 7        | 1    | (cypress adj semiconductor) and (dummy with trenches)   | EPO; JPO; DERWENT; IBM TDB | 2004/09/16 14:05 |
| 8        | 60   | (dummy with trenches) same (conductor or conductive or conducting or metal or polysilicon)                    | USPAT; US-PGPUB            | 2004/09/16 14:08 |
| 9        | 11   | ((dummy with trenches) same (conductor or conductive or conducting or metal or polysilicon)) and @ad<19980831 | USPAT; US-PGPUB            | 2004/09/16 14:07 |
| 10       | 22   | (dummy with trenches) same (conductor or conductive or conducting or metal or polysilicon)                    | EPO; JPO; DERWENT; IBM TDB | 2004/09/16 14:17 |
| 11       | 1    | ("6001733").PN.   | USPAT; US-PGPUB            | 2004/09/16 14:18 |
| 12       | 1    |   | USPAT                      | 2004/09/16 14:18 |
| 13       | 1    |   | USPAT                      | 2004/09/16 14:18 |
| 14       | 1    |   | USPAT                      | 2004/09/16 14:18 |
| 15       | 1    |   | USPAT                      | 2004/09/16 14:18 |
| 16       | 1    |   | USPAT                      | 2004/09/16 14:18 |
| 17       | 1    |   | USPAT                      | 2004/09/16 14:18 |

| L Number | Hits | Search Text   | DB              | Time stamp       |
|----------|------|---|-----------------|------------------|
| 1        | 1236 | 438/633,691,692,697,700.ccls. and @ad<19980831  | USPAT; US-PGPUB | 2004/09/21 10:10 |
| 2        | 627  | (438/633,691,692,697,700.ccls. and @ad<19980831) and (trench or hole or opening or recess or aperture) and (polishing or polish)  | USPAT; US-PGPUB | 2004/09/21 10:10 |
| 3        | 1091 | 257/752,774,775.ccls. and @ad<19980831  | USPAT; US-PGPUB | 2004/09/21 10:10 |
| 4        | 202  | (257/752,774,775.ccls. and @ad<19980831) and (trench or hole or opening or recess or aperture) and (polishing or polish)  | USPAT; US-PGPUB | 2004/09/21 10:11 |
| 5        | 193  | ((257/752,774,775.ccls. and @ad<19980831) and (trench or hole or opening or recess or aperture) and (polishing or polish)) not ((438/633,691,692,697,700.ccls. and @ad<19980831) and (trench or hole or opening or recess or aperture) and (polishing or polish)) | USPAT; US-PGPUB | 2004/09/21 10:11 |

DERWENT-ACC-NO: 2000-085654

DERWENT-WEEK: 200104

COPYRIGHT 1999 DERWENT INFORMATION LTD

TITLE: Forming a dual damascene structure  
for IC fabrication

INVENTOR: HUANG, Y; YANG, M ; YOU, T ; YEW, T

PATENT-ASSIGNEE: UNITED MICROELECTRONICS CORP[UNMIN]

PRIORITY-DATA: 1998TW-0110352 (June 26, 1998)

PATENT-FAMILY:

| PUB-NO          | PAGES | PUB-DATE          | MAIN-IPC |     |
|-----------------|-------|-------------------|----------|-----|
| US 6001733 A    |       | December 14, 1999 |          | N/A |
| 014             |       | H01L 021/44       |          |     |
| TW 396524 A     |       | July 1, 2000      |          | N/A |
| 000             |       | H01L 021/768      |          |     |
| JP 2000021879 A |       | January 21, 2000  |          | N/A |
| 009             |       | H01L 021/3205     |          |     |

APPLICATION-DATA:

| PUB-NO         | APPL-DATE | APPL-DESCRIPTOR  | APPL-NO |
|----------------|-----------|------------------|---------|
| US 6001733A    |           | N/A              |         |
| 1998US-0164856 |           | October 1, 1998  |         |
| TW 396524A     |           | N/A              |         |
| 1998TW-0110352 |           | June 26, 1998    |         |
| JP2000021879A  |           | N/A              |         |
| 1998JP-0313158 |           | November 4, 1998 |         |

INT-CL (IPC): H01L021/3205, H01L021/44 , H01L021/768

ABSTRACTED-PUB-NO: US 6001733A

BASIC-ABSTRACT:

NOVELTY - A dual damascene structure is formed for IC  
fabrication by forming

metal line trenches and a via hole in a dielectric layer as well as shallow dummy line trenches to decrease the area of an adhesion layer to be polished.

DETAILED DESCRIPTION - The method comprises:

- forming a first inter-metal dielectric layer and stop layer on a substrate;
- etching a via hole and dummy metal line pattern in the stop layer using a photoresist mask;
- adding a second inter-metal dielectric layer;
- pattern etching second and third metal line trenches and a via hole in the second dielectric layer, the second metal-line trench being above the first metal line and communicating with the via hole, the surface of the first metal line being exposed at the bottom of the via hole opening, and the third metal trench being beside the second metal line trench where no dummy metal line trench exists;
- adding an adhesion layer and a metal layer;
- and chemical-mechanical polishing to form the dual damascene structure.

USE - Forming a dual damascene with dummy metal lines.

ADVANTAGE - The dummy metal lines reduce the area of adhesion layer to be polished so that over-polishing of the metal lines is avoided. The thickness of the dummy metal lines is small so that parasitic capacitance is low.

DESCRIPTION OF DRAWING(S) - The drawing shows a dual damascene structure formed by the method of the invention.

First metal line 302

Shallow dummy metal lines 318a

Adhesion layer 328

Stop layer 306

Second metal line trench 322a

Inter-metal dielectric 317

Third metal line trenches 326

Via hole 324

CHOSEN-DRAWING: Dwg.3E/3

TITLE-TERMS: FORMING DUAL STRUCTURE IC FABRICATE

DERWENT-CLASS: L03 U11

CPI-CODES: L04-C13B;

EPI-CODES: U11-C05D3;

SECONDARY-ACC-NO:

CPI Secondary Accession Numbers: C2000-023888

Non-CPI Secondary Accession Numbers: N2000-067157